UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/526,394	03/16/00	HOWELL W	BU9-99-175

MMC2/0228

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EXAMINER	
FARFAN, N	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/28/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/526,394	Howell et al
Examiner	**Group Art Unit**
Nitin Parekh	2811

☒ Responsive to communication(s) filed on *Jan 18, 1901*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-21* is/are pending in the applicat

Of the above, claim(s) *15-21* is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-14* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al (US Pat. 4840302) in view of Chang et al (US Pat. 5048744) and Havemann (US Pat. 6156651).

Regarding claims 1 and 2, Gardner et al disclose a metallurgical structure in an integrated circuit (IC) /chip having underlying circuitry/components within an exterior covering comprising:

- a passivation layer/exterior covering (4 in Fig. 1; Col. 3)

- a via/hole (Col. 3, line 26; Fig. 1) through the passivation layer extending to a metal line (2 in Fig. 1)

- a barrier layer lining the via (12 in Fig. 1; Col. 3, line 43)

- metal layers/plug (14/16/18 in Fig. 1; Col. 3, line 63) in the via above the barrier layer comprising copper, the metal line comprising copper (Col. 3, line 18), and

- a solder bump/connector (1 in Fig. 1; Col. 4, line 13) formed on the metal layers/plug (Fig. 1; Col. 2, line 64- Col. 4, line 31).

Regarding claim 3, Gardner et al disclose the barrier layer comprising Ti and Cr but fail to specify the barrier layer comprising one or more layers of TiN, Ta and TaN. However, it is conventional in the chip packaging and interconnection technology art to use the materials such as Ti, Cr, Ta, TiN, etc. to improve the resistance against diffusion of impurities and improve adhesion. The admitted prior art (APA) specify using one or more layers of the materials such as Cr, W, Ti, etc. as a barrier layer. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the barrier layer comprising one or more layers of TiN, Ta and TaN to improve the resistance against diffusion of impurities in Gardner et al's structure as cited in claim 3.

Regarding claim 4, Gardner et al disclose using the barrier layer comprising Ti and Cr to improve the bond strength and reduce the contact resistance but fail to specify the use of the barrier layer to prevent the diffusion of elements within the solder bump into the metal line. However, the use of barrier layers such as Ti, Cr, etc. to provide the diffusion barrier against elements/impurities from solder and to improve adhesion, bond strength and reliability of the interconnection/solder joint is well-known in the chip packaging and interconnection technology art (see prior art disclosed by Gardner et al: Col. 1, line 51). Chang et al teach using Cr/Ti barrier layer to improve the diffusion/interaction and enhance conductivity between the solder and the metal such as copper (Col. 7, line 10; Col. 8, line 33; Fig. 8-11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the barrier layer

to prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Chang et al's teaching in Gardner et al's structure as cited in claim 4.

Regarding claim 5, Gardner et al disclose forming a planar surface on the passivation layer exterior of the metallurgical structure comprising barrier layer, metal plug and solder ball (Fig. 1; Col. 4, line 14).

Regarding claim 6, Gardner et al disclose the solder ball being in direct contact with the metal plug (Fig. 1; Col. 4, line 5).

Regarding claim 7, Gardner et al fail to specify a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball. Havemann teaches using conventional multilevel structure forming two levels of copper plugs/grooves with TiN barrier layer such that the second barrier layer is above the first metal plug and second metal plug is above the second barrier layer (Fig. 3G; Col. 4, line 55- Col. 5, line 38). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball to further prevent the diffusion of elements within the solder bump

into the metal line and to improve the reliability of the interconnection using Havemann's interconnection structure in Gardner et al's structure as cited in claim 7.

The combined teachings of Gardner et al (US Pat. 4840302), Havemann (US Pat. 6156651) and Chang et al (US Pat. 5048744) apply to claims 8-13 as explained above for claims 1-6 respectively.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

02-21-01

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER